FAIRCHILD
SEMICONDUCTOR ™

March 1988
Revised August 1999

74F657
Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and 3-STATE Outputs

General Description

The 74F657 contains eight non-inverting buffers with 3-STATE outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A Port and 64 mA at the B Port.

Features

- 300 Mil 24-pin slimline DIP
- Combines 74F245 and 74F280A functions in one package
- 3-STATE outputs
- B Outputs sink 64 mA
- 12 mA source current, B side
- Input diodes for termination effects

Ordering Code:

Order Number	Package Number	Package Description
75F657SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F657SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

IEEE/IEC

Connection Diagram
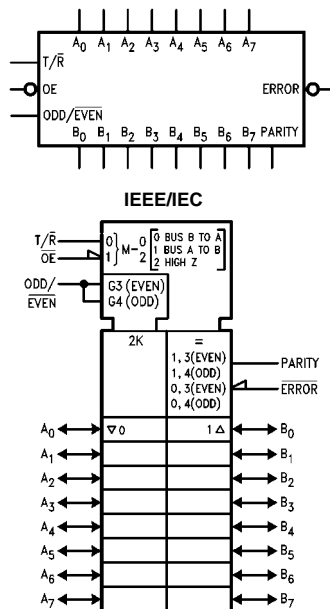
DS009584   www.fairchildsemi.com
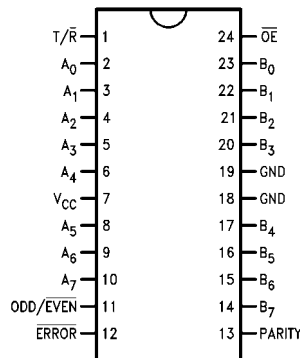
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_7	Data Inputs/	4.5/0.15	90 µA/− 90 µA
	3-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0-B_7	Data Inputs/	3.5/0.117	70 µA/−70 µA
	3-STATE Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)
$T/\overline{R}$	Transmit/Receive Input	2.0/0.067	40 µA/−40 µA
$\overline{OE}$	Enable Input	2.0/0.067	40 µA/−40 µA
PARITY	Parity Input/	3.5/0.117	70 µA/−70µA
	3-STATE Output	600/106.6 (80)	−12 mA/64 mA (48 mA)
ODD/$\overline{EVEN}$	ODD/$\overline{EVEN}$ Parity Input	1.0/0.033	20 µA/−20 µA
$\overline{ERROR}$	Error Output	600/106.6 (80)	−12 mA/64 mA (48 mA)

Functional Description

The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A Port to the B Port; Receive (active LOW) enables data from the B Port to the A Port.

The Output Enable ($\overline{OE}$) input disables the parity and $\overline{ERROR}$ outputs and both the A and B Ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting ($T/\overline{R}$ HIGH), the parity generator detects whether an even or odd number of bits on the A Port are HIGH and compares these with the condition of the parity select (ODD/$\overline{EVEN}$). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode ($T/\overline{R}$ LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then $\overline{ERROR}$ will be HIGH to indicate no error. If an odd number of bits on the B Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the $\overline{ERROR}$ will be LOW indicating an error.

Function Table

Number of Inputs that are HIGH	$\overline{OE}$	$T/\overline{R}$	ODD/$\overline{EVEN}$	Parity	$\overline{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Function Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram
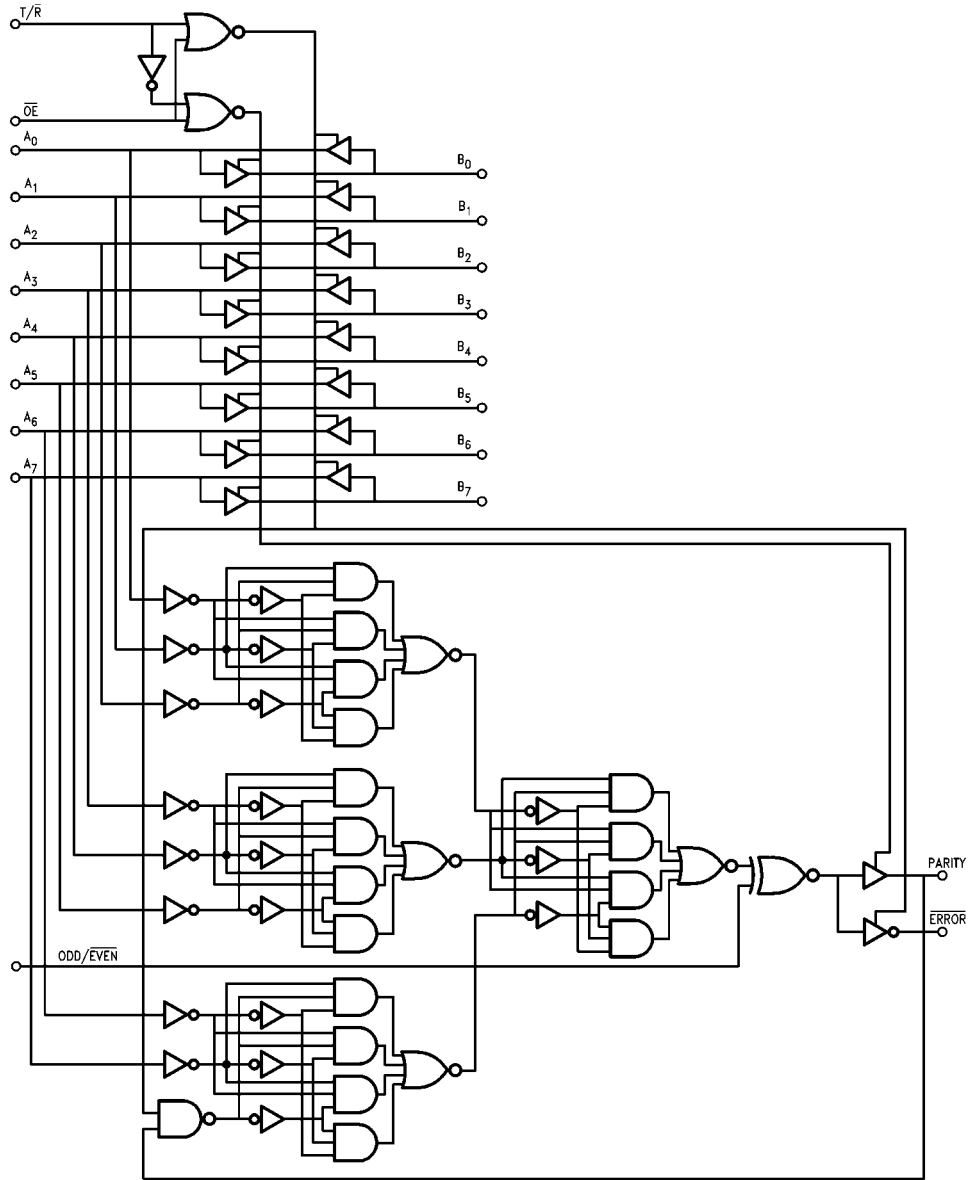
2 GROUND PINS
1 V_{CC} PIN

74F657

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.5					I_{OH} = −1 mA (A_n)
	Voltage	10% V_{CC}	2.4					I_{OH} = −3 mA (A_n B_n, Parity, $\overline{ERROR}$)
		10% V_{CC}	2.0			V	Min	I_{OH} = −15 mA (B_n, Parity, $\overline{ERROR}$)
		5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n, Parity, $\overline{ERROR}$)
V_{OL}	Output LOW	10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
	Voltage	10% V_{CC}			0.55	V	Min	I_{OL} = 64 mA (B_n Parity, $\overline{ERROR}$)
I_{IH}	Input HIGH				20			V_{IN} = 2.7V (ODD/$\overline{EVEN}$)
	Current				40	μA	Max	V_{IN} 2.7V (T/$\overline{R}$, $\overline{OE}$)
I_{BVI}	Input HIGH Current				100	μA	V_{CC} = 0	V_{IN} = 7.0V (T/$\overline{R}$, $\overline{OE}$, ODD/$\overline{EVEN}$)
	Breakdown Test							
I_{BVIT}	Input HIGH Current				1.0			V_{IN} = 5.5V (Parity, B_n)
	Breakdown Test (I/O)				2.0	mA	Max	V_{IN} = 5.5V (A_n)
I_{IL}	Input LOW				−20			V_{IN} = 0.5V (ODD/$\overline{EVEN}$)
	Current				−40	μA	Max	V_{IN} = 0.5V (T/$\overline{R}$, $\overline{OE}$)
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V ($\overline{ERROR}$)
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V ($\overline{ERROR}$)
$I_{IH} + I_{OZH}$	Output Leakage				70			$V_{I/O}$ = 2.7V (B_n, Parity)
	Current				90	μA	Max	$V_{I/O}$ = 2.7V (A_n)
$I_{IL} + I_{OZL}$	Output Leakage				−70			$V_{I/O}$ = 0.5V (B_n, Parity)
	Current				−90	μA	Max	$V_{I/O}$ = 0.5V (A_n)
I_{OS}	Output Short-Circuit		−60		−150			V_{OUT} = 0V (A_n)
	Current		−100		−225	mA	Max	V_{OUT} = 0V (B_n, Parity, $\overline{ERROR}$)
I_{CEX}	Output HIGH Leakage				250	μA	Max	V_{OUT} = V_{CC} ($\overline{ERROR}$)
	Current				1.0	mA	Max	V_{OUT} = V_{CC} (B_n, Parity)
					2.0	mA	Max	V_{OUT} = V_{CC} (A_n)
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n, Parity, $\overline{ERROR}$)
I_{CCH}	Power Supply Current			101	125	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			112	150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			109	145	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.5	8.0	2.5	9.5	2.5	9.0	ns
t_{PHL}	A_n to B_n, B_n to A_n	3.0	4.9	7.5	3.0	8.5	3.0	8.0	
t_{PLH}	Propagation Delay	6.5	10.1	14.0	5.5	18.0	6.0	16.0	ns
t_{PHL}	A_n to Parity	7.0	10.9	15.0	5.5	20.5	6.0	16.5	
t_{PLH}	Propagation Delay	4.5	7.8	11.0	4.0	14.0	4.0	13.0	ns
t_{PHL}	ODD/$\overline{EVEN}$ to PARITY	4.5	8.8	12.0	4.5	16.5	4.5	13.5	
t_{PLH}	Propagation Delay	4.5	7.5	11.0	4.0	14.0	4.0	13.0	ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERROR}$	4.5	8.2	12.0	4.5	16.5	4.5	13.5	
t_{PLH}	Propagation Delay	8.0	14.0	20.5	7.5	27.0	7.5	23.0	ns
t_{PHL}	B_n to $\overline{ERROR}$	8.0	15.0	21.5	7.5	28.5	7.5	23.5	
t_{PLH}	Propagation Delay	7.0	10.8	15.5	6.0	20.0	6.0	17.0	ns
t_{PHL}	PARITY to $\overline{ERROR}$	7.5	11.8	16.5	6.5	22.0	7.5	18.5	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	$\overline{OE}$ to A_n/B_n	4.0	6.5	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	$\overline{OE}$ to A_n/B_n	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	$\overline{OE}$ to $\overline{ERROR}$ (Note 3)	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	$\overline{OE}$ to $\overline{ERROR}$	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	$\overline{OE}$ to PARITY	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.6	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	$\overline{OE}$ to PARITY	1.0	5.1	7.5	1.0	8.5	1.0	8.0	

Note 3: These delay times reflect the 3-STATE recovery time only and not the signal time through the buffers or the parity check circuity. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output after the $\overline{ERROR}$ pin has been enabled (Output Enable times). VALID data at the $\overline{ERROR}$ pin $\geq$ (A to PARITY) + (Output Enable Time).
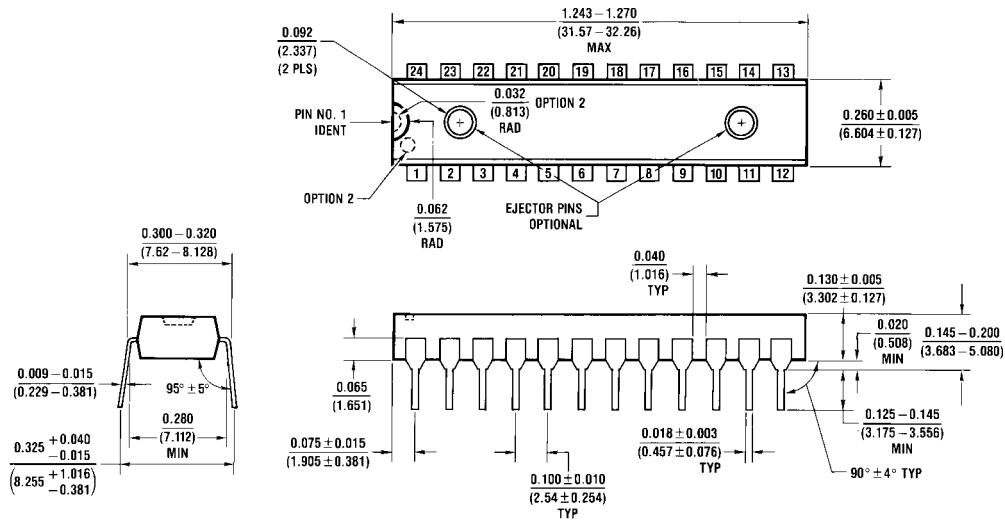
Physical Dimensions inches (millimeters) unless otherwise noted
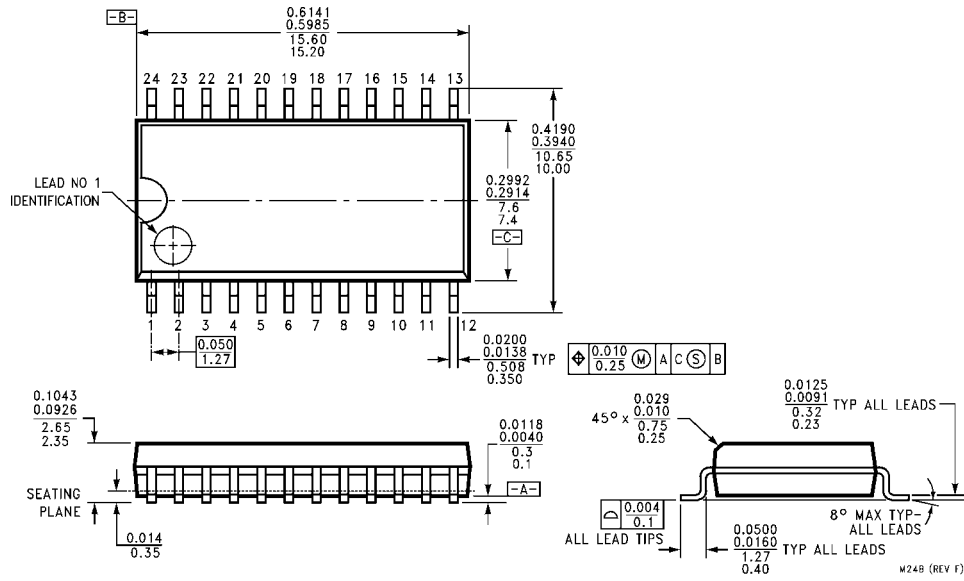
24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.092
(2.337)
(2 PLS)

1.243 − 1.270
(31.57 − 32.26)
MAX

PIN NO. 1
IDENT

0.032
(0.813)
RAD
OPTION 2

0.260 ± 0.005
(6.604 ± 0.127)

OPTION 2

0.062
(1.575)
RAD

EJECTOR PINS
OPTIONAL

0.300 − 0.320
(7.62 − 8.128)

0.040
(1.016)
TYP

0.130 ± 0.005
(3.302 ± 0.127)

0.020
(0.508)
MIN

0.145 − 0.200
(3.683 − 5.080)

0.009 − 0.015
(0.229 − 0.381)

95° ± 5°

0.065
(1.651)

0.125 − 0.145
(3.175 − 3.556)
MIN

0.280
(7.112)
MIN

0.075 ± 0.015
(1.905 ± 0.381)

0.018 ± 0.003
(0.457 ± 0.076)
TYP

$0.325 \begin{smallmatrix} +0.040 \\ -0.015 \end{smallmatrix}$

$\left(8.255 \begin{smallmatrix} +1.016 \\ -0.381 \end{smallmatrix} \right)$

0.100 ± 0.010
(2.54 ± 0.254)
TYP

90° ± 4° TYP

N24C (REV F)

24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

www.fairchildsemi.com